

Proposal to Investigate Silicon CMOS

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Physics Motivation

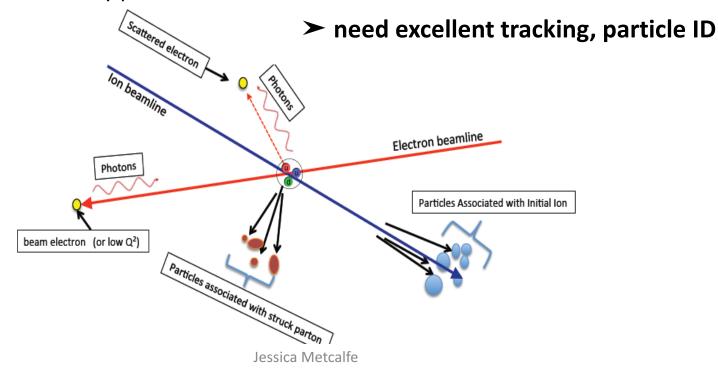


Physics Goals of the EIC:

- Understand the nature of the gluon structure
- Measure nucleon and nuclear structure
 - includes transverse and flavor structure

To Achieve the Physics Goals of the EIC:

- Measure the transverse momentum dependent parton distributions (TMDs)
- Measure the heavy flavor production in deep inelastic scattering and the related charm and beauty parton distributions



EIC Tracking

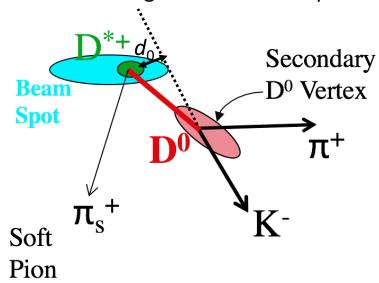


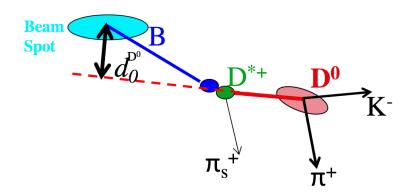
Tracking Requirements:

- Secondary vertex reconstruction
- Impact Parameter Resolution, d_0
- Small pixels for high position resolution
- Low mass budget to avoid secondary interactions

particle	ст
π±	7.8 m
π0	25 nm
K±	3.7 m
KOS	2.7 cm
KOL	15.3 m
D±	312 μm
D0	123 μm

Particles resulting from the struck parton:





Example Performance



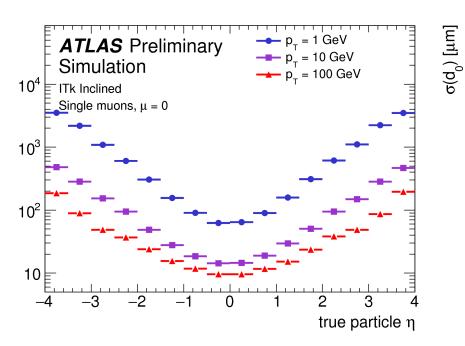
Example:

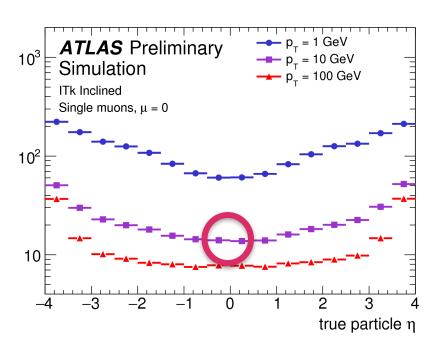
ATL-PHYS-PUB-2016-025

ATLAS ITK Upgrade with 50 μm x 50 μm pixels

- Includes high pileup -> not a factor at the EIC
- Expect further improvement

 $\sigma(z_0)$ [μm]





- Excellent impact parameter performance
- d_0 <30 μm for $|\eta|$ < 3.5 , < 50 μm for $|\eta|$ < 4 for p_T = 10 GeV muons
- $z_0 < 300 \ \mu m$ for $|\eta| < 3.5$, < 450 μm for $|\eta| < 4$ for $p_T = 10$ GeV muons

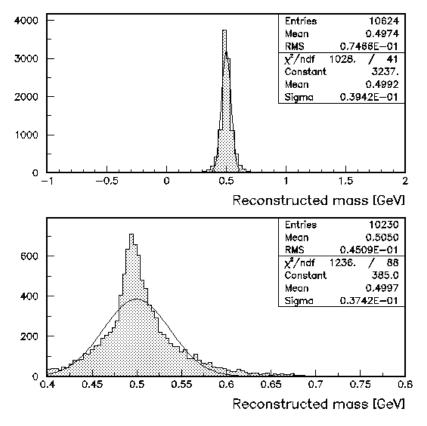
Particle ID

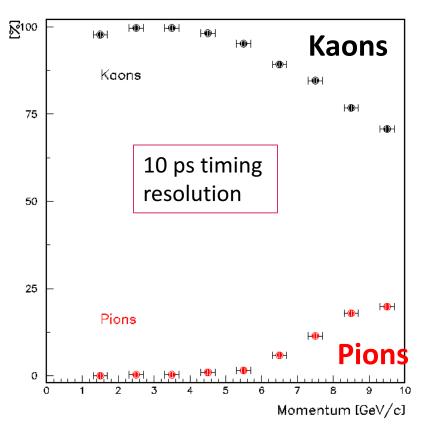


Time of Flight for Particle ID

Preliminary Results from Argonne EIC Simulation Group:

- Time information associated with each particle in the silicon tracker and EM calorimeter using a single particle gun and an SiD detector
- Timing resolution of 10 ps allows for excellent kaon-pion separation

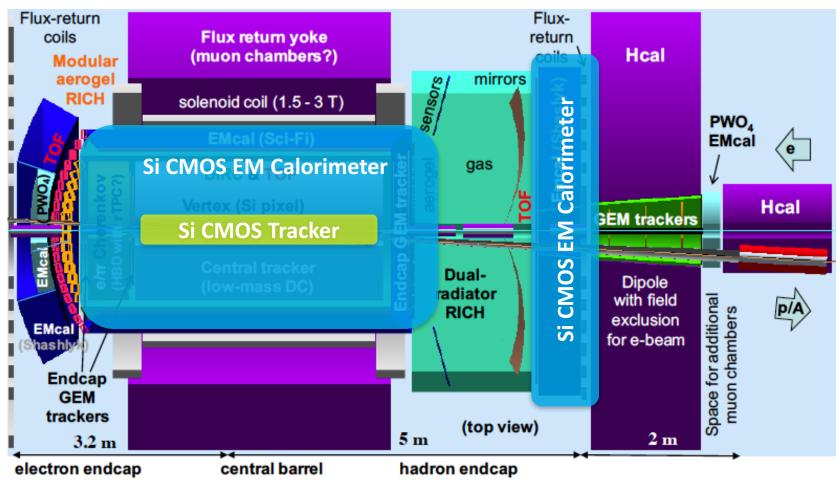




Example EIC Detectors



A proposed JLab Detector for the EIC:



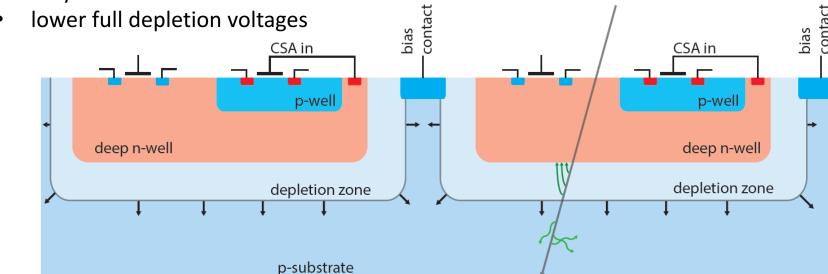
Propose to investigate monolithic CMOS technologies that can provide necessary position resolution (Tracker) and particle ID (EM Calorimeter, Forward EM Calorimeter)

Monolithic CMOS



Monolithic HVCMOS

- Under consideration for the ATLAS Phase II pixel detector upgrade
- Less expensive by x2 than traditional silicon sensors
- Integrated sensor + signal amplification
- Use commercially available CMOS processing with a few modifications
 - Deep n-well to isolate on-pixel electronics
 - high resistivity substrates for high voltage without breakdown
- Timing is currently ~1-100 ns
 - collect by drift, not diffusion
- pixel sizes down to at least 50 μm x 50 μm
- fully monolithic reduces material



CMOS @ AMS foundry



ams 0.35 μm/180 nm

Key features:

Technology node 0.35 μm/180 nm

Wells No possibility of isolating n-wells from

the collecting deep n-well. No CMOS

electronics in the sensor area.

Can induce cross-talk.

- Metal layers 4/6

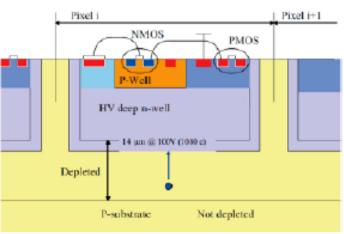
HR 20 (standard value) – 1k Ω·cm (since 2015/6)

- **HV** -150 V < HV < 0 V

- Depletion region 140 μm thick

Backside biasing Not possible

Stitching Not possible

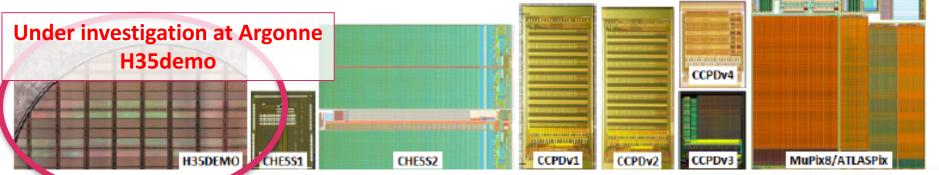


I. Peric, NIMA 650 pp. 158-162, 2011

Prototypes:

ams 0.35 μm → Initial R&D developments, H35CCPDv1-2, H35DEMO, HVStrip, CHESS1-2 (strips)

ams 180 nm → CCPDv1-8, CLICpix=CCPDv3, C3PD, MuPix1-8 (Mu3e), MuPix8/ATLASPix_®



CMOS: H35demo



HVCMOS sensor

Monolithic matrices

Capacitively coupled to FEI4

(glued)

Resistivities:

- 20 Ω
- 80 Ω
- 200 Ω
- 1000 Ω

Thickness:

- 300 μm
- 100 μm

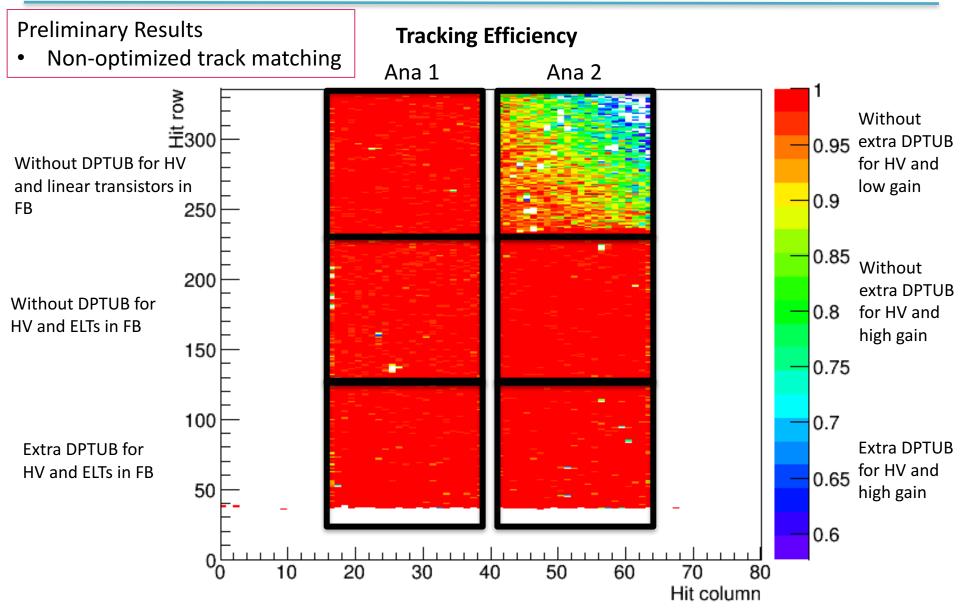
Bias Voltage

- Top side
- Back side (separate process from AMS)



CMOS: H35demo





CMOS Investigation for the EIC



Proposal:

- Characterization measurements of CMOS pixel structures relevant to the EIC
 - Timing
 - thinned sensors
 - Back-side bias voltage
 - Optimized designs (comparators, amplifiers, high gain, etc.)
 - H35demo, H18 (MuPix8/ATLASPix)
- Include pixel geometries relevant to the EIC in the next design submissions
 - Rely on input from Argonne EIC simulations group
- Leverage ongoing work in Argonne HEP in this area

Toward 10 ps Timing Resolution:

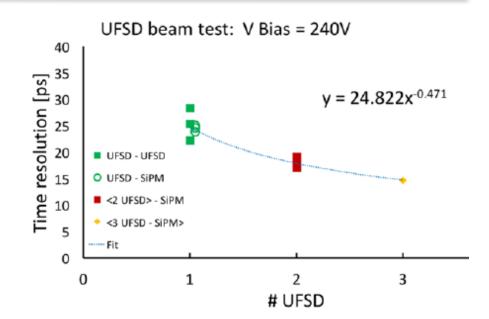
- Work with CMOS designer, Ivan Peric, to develop a design
 - CMOS plus a gain layer similar to that in an LGAD silicon sensor
 - Use TCAD simulation to demonstrate potential
 - Determine how these technologies would benefit an EIC detector

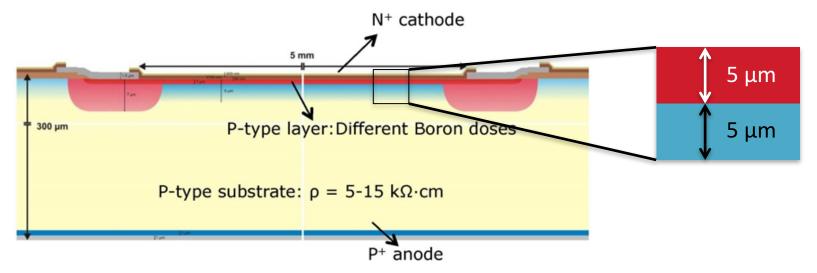
Low Gain Amplifying Detectors (LGAD)



LGAD

- amplification region, ~5 μm thick
 - thin layer of Boron or Gallium
 - modifies the effective doping concentration profile -> electric field profile to create high field gradient
- Radiation tolerance shown up to 10^{14} n_{eq}/cm^2
 - not as tolerant as traditional silicon due to the high reactivity of the accelerant layer

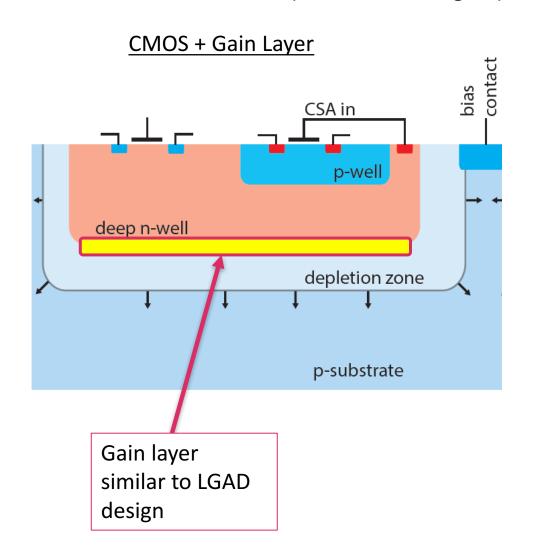




Fast CMOS



Discussions with Ivan Peric (AMS CMOS designer):



- Possible foundries:
 - AMS, Lfoundry
- May be possible to include a gain layer in the next AMS MPW run
- Need to add to the TCAD simulations
 - Understand constraints on pixel size

Project Deliverables



- 1) The postdoc will carry out test bench measurements in the lab at Argonne as well as test beam measurements at Fermilab and/or CERN. These include:
 - Characterization of design options for an EIC
 - Precision timing measurements of charge collection properties
 - Test beam performance measurements with particle species and energies specific to the EIC
- 2) The postdoc will also perform TCAD simulations using an existing license at Argonne.
 - TCAD simulations of existing samples will be set up at Argonne
 - TCAD simulation results will be compared to measurements
 - An iterative process will aim at identifying the underlying cause of any discrepancies and the simulation will be corrected
- 3) The postdoc will work with our collaborating design engineers to identify modifications in simulation toward a design optimized for timing precision at the EIC.



Budget	Postdoc Salary	Design Engineer		Total Cost
Scenarios	(\$k)	(\$k)	Travel (\$k)	(\$k)
Nominal	\$125	\$30	\$0	\$155
-20%	\$125	\$0	\$0	\$125
-40%	\$93	\$0	\$0	\$93

- The nominal budget will complete all three deliverables in the first year.
- The nominal budget minus 20% will complete deliverable items 1-2 since the third item requires compensation for a design engineer and this funding would be dropped first.
- The nominal budget minus 40% will complete only the first deliverable using 0.75 FTE of the postdoc the other 0.25 FTE would be funded for different work under the EIC LDRD program.



Thank You

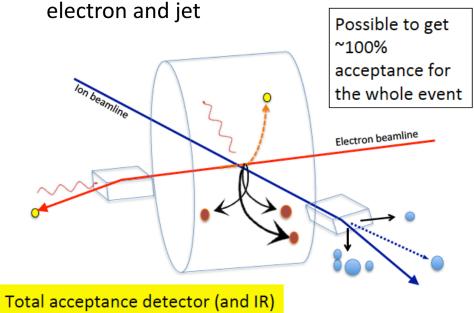
EIC Physics

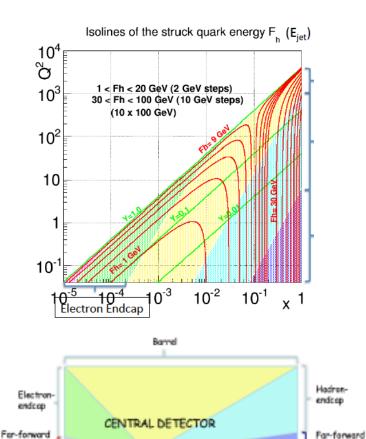


Measure x and Q²

- x: measure of the momentum fraction of the struck quark in a proton
- Q²: measure of the resolution

via energy and angle of scattered





Rik Yoshida EIC Detector R&D meeting July 2016

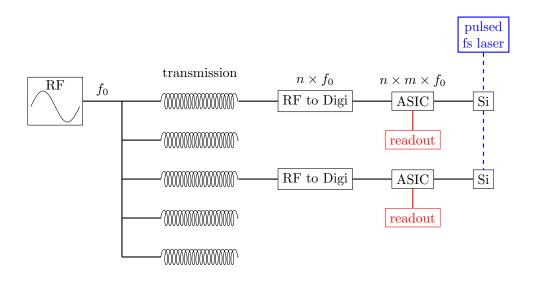
➤ need excellent tracking, particle ID

Timing Synchronization



Separate Argonne Effort on Detector-Wide Timing Synchronization:

- Goal is to maintain the integrity of the clock between detectors
- requires maintaining low phase noise/jitter from a single reference signal
- Strategy is to use an RF clock



CMOS Concept for EIC



Luminosity

- up to 10^{34}
- expect <0.1 interactions per event
 - Pileup should not be an issue, still need to identify primary vertex
- Bunch crossing ~10 ns
 - Fast readout or time stamp to identify bunch crossing for an event

Vertexing

- Hadron beam spot $\beta = 5$ cm
- Low material budget

Particle identification

- time of flight
- dE/dx

Radiation damage

- $<1 \times 10^{10} \text{ 1 MeV n}_{eq}/\text{cm}^2$
 - Not an issue for most silicon technologies

Material Budget

Keep as low as possible

Monolithic SiGe for EIC



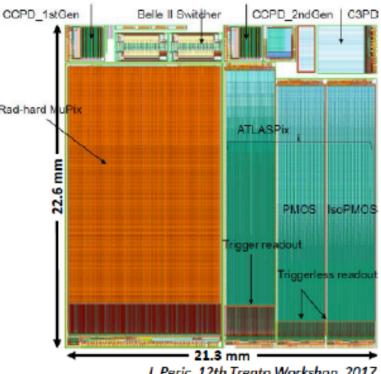
ams 180 nm - MuPix8/ATLASPix and new design

MuPix8/ATLASPix:

- Submitted in January 2017 (eng. run)
- It includes:
 - Matrices of pixels for ATLAS
 - Pixel size: 25 μm x 25 μm, 25 μm x 50 μm, 33 μm x 125 μm, Rad-hard NuPix 50 μm x 60 μm, 40 μm x 125 μm
 - MuPix8
 - Pixel size: 80 μm x 81 μm
 - Matrix with 200 x 128 pixels
 - Pixels with CSA and output driver only
 - Hit info: x-address, y-address, 10-bit TS, 6-bit amplitude
 - Time resolution: 6.25 ns
 - Nominal power consumption: 300 mW per matrix
 - Hit driven, triggerless R/O (MuPix8, Simple ATLASPix)
 - Triggered R/O (M ATLASPix)
 - Resistivity: $20 \Omega \cdot \text{cm}$, $50\text{-}100 \Omega \cdot \text{cm}$, $100\text{-}400 \Omega \cdot \text{cm}$, 600-1.1k Ω·cm

New design:

Studies considering the integration of RD53-like periphery logic



I. Peric, 12th Trento Workshop, 2017



Advantages of SiGe Bipolar Over CMOS for Silicon Strip Detectors

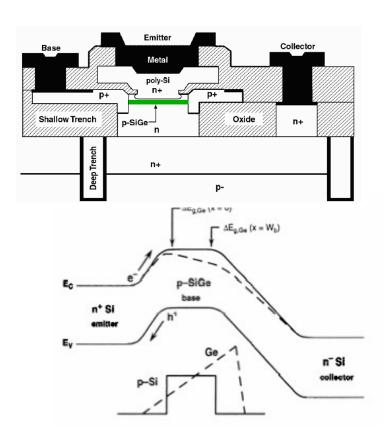
- A key element in the design of low noise, fast shaping, charge amplifiers is high transconductance in the first stage.
- With CMOS technologies, this requires relatively larger bias currents than with bipolar technologies.
- The changes that make SiGe Bipolar technology operate at 100 GHz for the wireless industry coincide with the features that enhance performance in high energy particle physics applications.
 - Small feature size increases radiation tolerance.
 - Extremely small base resistance (of order 10-100 Ω) affords low noise designs at very low bias currents.
- These design features are important for applications with:
 - Large capacitive loads (e.g. 5-15 pF silicon strip detectors)
 - Fast shaping times (e.g. accelerator experiments with beam crossing times of tens of nanoseconds in order to identify individual beam crossing events)

Monolithic SiGe for EIC



Second Option:

- Monolithic (CMOS-like) design based in SiGe HBT technology
 - Faster than CMOS due to band-gap engineering



TT PET results presented at TIPP 2017:

